File 2:INSPEC 1969-2002/Mar W1
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Set	Items	Description
S1	834	SILICON ON INSULATOR METAL OXIDE SEMICONDUCTOR OR SOI(W) MOSFET
S2	55	(SILICON(2N)INSULATOR()METAL(2N)MOSFET) OR (SOI(2N)METAL()OXIDE()SEMICONDUCTOR)
S3	849	SILICON()ON()INSULATOR()METAL()OXIDE()SEMICONDUCTOR OR SOI(W) MOSFET
S4	45	(S2 OR S3) NOT S1
S5	10	S4 AND ((BURY??? OR BURIED OR ENCAPSUL? OR CAPSUL? OR ENCAS?????)(3N)(INSULAT? OR DIELECTRIC OR OXIDE))

03/08/2002

5/3,AB/1
DIALOG(R)File 2:INSPEC

7117431 INSPEC Abstract Number: B2002-01-2560R-058
Title: Silicon-on-insulator MOSFET structure for sub-100 nm channel regime and performance perspective
Author(s): Omura, Y.
Author Affiliation: High-Technol. Res. Center, Kansai Univ., Osaka, Japan
Journal: Journal of the Electrochemical Society vol.148, no.12 p. G746-9
Publisher: Electrochem. Soc,
Publication Date: Dec. 2001 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
SICI: 0013-4651(200112)148:12L.g746:SIMS;1-0
Material Identity Number: J010-2001-014
U.S. Copyright Clearance Center Code: 0013-4651/2001/148(12)/746/4/$7.00
Language: English
Abstract: This paper describes performances of the partial-ground-plane (PGP) **silicon-on-insulator metal-oxide semiconductor** field effect transistor aiming at the demanding radio-frequency applications of the future. In the PGP device, short-channel effects are suppressed by terminating most of the source- and drain-induced electric fields to small heavy doping regions that are localized below the source and drain regions. As a result, the sub-100 nm PGP device with appropriately designed heavy doping regions minimizes the influence of the source and drain parasitic capacitance, even if thin **buried oxide** layers are used.
Subfile: B

5/3,AB/2
DIALOG(R)File 2:INSPEC

6927583 INSPEC Abstract Number: B2001-06-7230G-059
Title: A low voltage hybrid bulk/SOI CMOS active pixel image sensor
Author(s): Chen Xu; Weiquan Zhang; Chan, M.
Author Affiliation: Dept. of Electr. & Electron. Eng., Hong Kong Univ. of Sci. & Technol., China
Journal: IEEE Electron Device Letters vol.22, no.5 p.248-50
Publisher: IEEE,
Publication Date: May 2001 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(200105)22:5L.248:VHBC;1-J
Material Identity Number: I338-2001-005
U.S. Copyright Clearance Center Code: 0741-3106/2001/$10.00
Language: English
Abstract: A hybrid bulk/silicon-on-insulator (**SOI**) complementary **metal oxide semiconductor** (CMOS) active pixel image sensor has been fabricated and studied. The active pixel comprised of reset and source follow transistors on the SOI thin film while the photodiode is fabricated on the SOI handling substrate after removing the **buried oxide** . The bulk photodiode can be optimized for efficiency with the use of lightly doped SOI substrate without compromising the circuit performance. On the other hand, the elimination of wells on the SOI thin-film allows the use of PMOSFET without increasing the pixel size. The addition of a PMOSFET in the active pixel structure can reduce the minimum

operating voltage of the circuit beyond that of conventional designs. With the combination of the high quantum efficiency of bulk photodiode and the low power advantage of SOI technology, the hybrid technology is attractive for scaled low voltage imaging applications.
Subfile: B

5/3,AB/3
DIALOG(R)File 2:INSPEC

6206160 INSPEC Abstract Number: B1999-05-2560R-021
Title: Effects of **buried oxide** on electrical performance of thin-film **silicon-on-insulator metal-oxide-semiconductor** field-effect transistor
Author(s): Jong-Wook Lee; Min-Rok Oh; Yo-Hwan Koh
Author Affiliation: Div. of Semicond. Res., Hyundai Electron. Ind. Co. Ltd., Ichon, South Korea
Journal: Journal of Applied Physics vol.85, no.7 p.3912-15
Publisher: AIP,
Publication Date: 1 April 1999 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
SICI: 0021-8979(19990401)85:7L.3912:EBOE;1-H
Material Identity Number: J004-1999-005
U.S. Copyright Clearance Center Code: 0021-8979/99/85(7)/3912(4)/$15.00
Language: English
Abstract: Local oxidation of silicon-isolated thin-film silicon-on-insulator (SOI) device characteristics have been investigated in terms of stress in the **buried-oxide** interface by both simulation and experiment. A bonded SOI wafer with a 400 nm **buried oxide** and a separation by implanted oxygen SOI wafer with a 100 nm **buried oxide** are used for device fabrication. In the 100 nm **buried-oxide** case, boron atoms are accumulated at the silicon side in the interface between the silicon film and oxide (i.e., including the **buried oxide** and field **oxide**) due to a highly stressed oxide so that the increased boron concentration increases the threshold voltage of the edge channel. Therefore, it is found that there is no drain current hump in the subthreshold region of thin-film **SOI** n-channel **metal-oxide-semiconductor** field-effect transistors with 100 nm **buried oxide**. From the simulation, it is demonstrated that the 100 nm **buried oxide** has higher compressive stress than the 400 nm counterpart after the local oxidation of silicon process.
Subfile: B

5/3,AB/4
DIALOG(R)File 2:INSPEC

5897215 INSPEC Abstract Number: B9806-2560R-005
Title: Physical origin and characteristics of gate capacitance in silicon metal-oxide-semiconductor field-effect transistors
Author(s): Nakajima, Y.; Horiguchi, S.; Shoji, M.; Omura, Y.
Author Affiliation: NTT Basic Res. Labs., Kanagawa, Japan
Journal: Journal of Applied Physics vol.83, no.9 p.4788-96
Publisher: AIP,

Publication Date: 1 May 1998 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
SICI: 0021-8979(19980501)83:9L.4788:POCG;1-M
Material Identity Number: J004-98008
U.S. Copyright Clearance Center Code: 0021-8979/98/83(9)/4788(9)/$15.00
Language: English

Abstract: The physical origin of gate capacitance in both bulk and silicon-on-insulator (SOI) metal-oxide-semiconductor%%
% field-effect transistors (MOSFETs) is studied. The gate capacitance is theoretically derived as the series capacitance comprising the oxide capacitance, number capacitance (C/sub N/), level capacitance (C/sub level/), and field capacitance (C/sub field/). C/sub N/ is in proportion to the thermodynamic density of states under the hypothetical condition that the subband energy levels remain constant when the total electron density is differentiated by the Fermi level. C/sub level/ is inversely proportional to the result of differentiating the subband energy level by the total electron density. In the case of bulk MOSFETs or SOI MOSFETs with thick buried oxide , C/sub field/, which originates from the electric field at the edge of the depletion layer, is negligible. In addition to the fact that our new theoretical model corresponds to the intuitive conventional model expressed in terms of the effective thickness of the inversion layer in bulk MOSFETs, it is demonstrated that the conventional capacitance model is also applicable to SOI MOSFETs at 300 K. We have calculated self-consistently the capacitance of a bulk MOSFET and of SOI MOSFETs with various top-silicon layer thicknesses at 300 K. At the fixed total electron density near 10/sup 12/ cm/sup -2/, the gate capacitance becomes large with decreasing top-silicon layer thickness. This difference in the gate capacitance mainly comes from C/sub level/, which means that in the case of SOI MOSFETs with a thin top-silicon layer, a small increase in the subband energy level with increasing electron density results in large gate capacitance and high performance of the SOI MOSFETs at 300 K.

Subfile: B

5/3,AB/5
DIALOG(R)File 2:INSPEC

5830081 INSPEC Abstract Number: B9803-2560R-075
Title: Effects of buried oxide stress on thin-film silicon-on-insulator metal-oxide-semicondu
ctor field-effect transistor
Author(s): Jong-Wook Lee; Myung-Hee Nam; Jeong-Hee Oh; Ji-Woon Yang; Won-Chang Lee; Hyung-Ki Kim; Min-Rok Oh; Yo-Hwan Koh
Author Affiliation: Div. of Semicond. Res., Hyundai Electron. Ind. Co. Ltd., Kyoungki, South Korea
Journal: Applied Physics Letters vol.72, no.6 p.677-9
Publisher: AIP,
Publication Date: 9 Feb. 1998 Country of Publication: USA
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(19980209)72:6L.677:EBOS;1-M
Material Identity Number: A135-98007
U.S. Copyright Clearance Center Code: 0003-6951/98/72(6)/677(3)/$15.00
Language: English
Abstract: Thin-film silicon-on-insulator (SOI) device characteristics have been investigated in terms of stress in the buried oxide interface by both simulation and experiment. Bonded SOI wafer with a 400 nm

buried oxide and SOI wafer with a 100 nm buried oxide which is made by implanted oxygen are used as a substrate for device fabrication. From the simulation, it is demonstrated that the 100 nm buried oxide has higher compressive stress than the 400 nm counterpart after the local oxidation of silicon process. With the highly compressive-stressed buried oxide, boron atoms may accumulate at the silicon side, especially at the silicon edge, under tensile stress so that these accumulated boron atoms increase threshold voltage of the edge channel. Therefore, it is found that there is no hump of the drain current in the subthreshold drain current-gate-voltage characteristics of thin-film SOI n-channel metal-oxide-semiconductor field-effect transistors (MOSFET) with the highly compressed buried oxide.

Subfile: B

? T S5/3,AB/6-10

5/3,AB/6

DIALOG(R)File 2:INSPEC

5824998 INSPEC Abstract Number: B9803-2560R-054

Title: The influence of the buried oxide defects on the gate oxide reliability and drain leakage currents of the silicon-on-insulator metal-oxide-semiconductor field-effect transistors

Author(s): Iwamatsu, T.; Ipposhi, T.; Yamaguchi, Y.; Imai, Y.; Maegawa, S.; Tsubouchi, N.; Nishimura, T.

Author Affiliation: ULSI Lab., Mitsubishi Electr. Corp., Hyogo, Japan

Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) vol.36, no.12A p.7104-9

Publisher: Publication Office, Japanese Journal Appl. Phys,

Publication Date: Dec. 1997 Country of Publication: Japan

CODEN: JAPNDE ISSN: 0021-4922

SICI: 0021-4922(199712)36:12AL.7104:IBOD;1-4

Material Identity Number: F221-98001

Language: English

Abstract: The relation between gate oxide and buried oxide (BOX) integrity was investigated for several silicon on insulator (SOI) materials. The yield values of the gate oxide breakdown were found to depend on the BOX leakage currents. The gate leakage currents and BOX leakage currents were observed at the same location by optical luminescence. Scanning electron microscope (SEM) observations of the luminescence in the low-dose implanted oxygen separation region of the (SIMOX) substrate, showed that the SOI layer had disappeared, and voids appeared in the BOX layer. In addition, Q/sub bd/ of the gate oxide was low in capacitors where the BOX leakage currents were observed. It is thought that the crystalline quality of the SOI layer on the imperfect BOX layer was degraded, causing the gate leakage currents. Moreover, it was observed that the yield value of the drain leakage currents of the SOI metal-oxide-semiconductor field-effect transistors (MOSFET's) also depended on the BOX leakage currents.

Subfile: B

5/3,AB/7

DIALOG(R)File 2:INSPEC

5639582 INSPEC Abstract Number: B9709-2560R-003
Title: Effect of buried oxide thickness in a thin-film silicon on insulator power metal-oxide-semiconductor field-effect transistor
Author(s): Matsumoto, S.; Yachi, T.
Author Affiliation: NTT Integrated Inf. & Energy Syst. Labs., Musashino, Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) vol.36, no.6A p.3438-42
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: June 1997 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(199706)36:6AL.3438:EBOT;1-9
Material Identity Number: F221-97012
Language: English
Abstract: Effect of buried oxide thickness in a thin-film silicon on insulator (SOI) power metal-oxide-semiconductor field effect (MOSFET) transistor is demonstrated. In the thin-film SOI power MOSFETs fabricated on a separation by implanted oxygen (SIMOX) substrate, devices with a thin buried oxide showed higher performance than ones with a thick buried oxide. The device with thinner top silicon layer operated in a fully depleted mode. The minimum specific on-resistance of the fabricated device was 66 m Omega .mm/sup 2/ at a breakdown voltage of 32 V.
Subfile: B

5/3,AB/8
DIALOG(R)File 2:INSPEC

4941832 INSPEC Abstract Number: B9506-2560R-016
Title: Switching characteristics of a thin film SOI power MOSFET
Author(s): Matsumoto, S.; Il-Jung Kim; Sakai, T.; Fukumitsu, T.; Yachi, T.
Author Affiliation: Interdisciplinary Res. Labs., NTT, Tokyo, Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers & Short Notes) vol.34, no.2B p.817-21
Publication Date: Feb. 1995 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
Conference Title: 1994 International Conference on Solid State Devices and Materials (SSDM '94)
Conference Date: 23-26 Aug. 1994 Conference Location: Kanagawa, Japan
Language: English
Abstract: This paper describes switching characteristics of thin film silicon-on-insulator (SOI) power metal-oxide-semiconductor field-effect transistors (MOSFETs) based on the results of numerically simulating thin-film SOI power MOSFETs in the 50-V class. The dependence of the rise time and fall time on the doping concentration of the substrate, on the doping type of the substrate, and on the thickness of the buried oxide layer are studied. In addition, the optimum device structure of the thin-film SOI power MOSFET for high-frequency switching application is also described.
Subfile: B

5/3,AB/9
DIALOG(R)File 2:INSPEC

4901033 INSPEC Abstract Number: B9504-2560R-068
Title: Analysis of SIMOX metal-oxide-semiconductor transistors operated in the high temperature range
Author(s): Ouisse, T.; Reichert, G.; Cristoloveanu, S.; Faynot, O.; Giffard, B.
Author Affiliation: Lab. de Phys. des Composants a Semicond., CNRS, Grenoble, France
Journal: Materials Science & Engineering B (Solid-State Materials for Advanced Technology) vol.B29, no.1-3 p.21-3
Publication Date: Jan. 1995 Country of Publication: Switzerland
CODEN: MSBTEK ISSN: 0921-5107
U.S. Copyright Clearance Center Code: 0921-5107/95/$9.50
Conference Title: High Temperature Electronics: Materials, Devices and Applications. Symposium E at the E-MRS Spring Meeting 1994
Conference Date: 24-27 May 1994 Conference Location: Strasbourg, France
Language: English
Abstract: A systematic investigation of the physical properties and performance of SIMOX silicon-on-insulator (SOI) metal-oxide-semiconductor field effect transistors, operated from 210 to 625 K is presented. It is shown that SOI devices are attractive candidates for minimizing leakage currents at high temperature. The surface mobility follows conventional behaviour. The sensitivity of the SIMOX buried oxide to hot carrier injection is found to exhibit a maximum at an intermediate temperature, around 400 K.
Subfile: B

5/3,AB/10
DIALOG(R)File 2:INSPEC

4654413 INSPEC Abstract Number: B9406-2560R-012
Title: Device simulation of a thin-film silicon on insulator power metal-oxide-semiconductor field-effect transistor for structure optimization
Author(s): Matsumoto, S.; Yoshino, H.
Author Affiliation: NTT Interdisciplinary Res. Labs., Tokyo, Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers & Short Notes) vol.33, no.1B p.519-23
Publication Date: Jan. 1994 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
Conference Title: 1993 International Conference on Solid State Devices and Materials (SSDM '93)
Conference Sponsor: Japan Soc. Appl. Phys
Conference Date: 29 Aug.-1 Sept. 1993 Conference Location: Chiba, Japan
Language: English
Abstract: The authors propose an optimised device structure based on the results of numerically simulating thin-film silicon on insulator (SOI) power metal-oxide-semiconductor field-effect transistors (MOSFETs) in the 50-V class. The dependence of the breakdown voltage and specific on-resistance on the doping concentration of the drain offset region, on the thickness of the superficial silicon layer, on the

thickness of the buried oxide layer, and on the drain offset length are compared for buried channel MOSFETs and surface channel MOSFETs.
Subfile: B